IN THE CLAIMS

1. (Previously Presented) A semiconductor device having an electrically erasable programmable read only memory (EEPROM) array including rows and columns of memory cells comprising:

a first well region and a second well region within a semiconductor substrate, wherein the first well region and the second well region are spaced apart and electrically isolated;

a first column of memory cells positioned within the first well region;

a second column of memory cells positioned within the second well region;

a first tunnel dielectric of a first memory cell in the first column of memory cells and a second tunnel dielectric of a second memory cell in the second column of memory cells, wherein the first and second memory cells are devoid of floating gates;

a first charge storage layer of the first memory cell formed over the first tunnel dielectric and a second charge storage layer of the second memory cell formed over the second tunnel dielectric;

a first control gate of the first memory cell formed over the first charge storage layer and a second control gate of the second memory cell formed over the second charge storage layer, wherein the first control gate and the second control gate are in a same row and electrically coupled via a common wordline;

a first bitline electrically coupled to drain regions of each memory cell in the first column of memory cells,

a second bitline electrically coupled to drain regions of each memory cell in the second column of memory cells;

a first source line electrically coupled to source regions of each memory cell in the first column of memory cells, wherein the first source line and a source region of at least one memory cell in the first column of memory cells are electrically coupled to the first well region; and

a second source line electrically coupled to source regions of each memory cell in the second column of memory cells, wherein the second source line, and a source

region of at least one memory cell in the second column of memory cells is electrically coupled to the second well region.

2. (Original) The semiconductor device of claim 1, wherein the first and second well regions are p-wells.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The semiconductor device of claim [[4]] 1, wherein the first and second charge storage layers comprise nitrogen.

6. (Original) The semiconductor device of claim 5, wherein the fist and second charge storage layers are selected from the group consisting of silicon nitride and silicon oxynitride.

7. (Original) The semiconductor device of claim 1, further comprising:
a first blocking layer of the first memory cell formed over the first charge storage layer and under the first control gate and a second blocking layer of the second memory cell formed over the second charge storage layer and under the first control gate.

8. (Original) The semiconductor device of claim 1, wherein the first well region and the second well region are spaced apart and electrically isolated by a trench isolation feature.

9. (Original) The semiconductor device of claim 8, further comprising a third well region below the shallow trench isolation feature that electrically isolates the first well region from the second well region, wherein the first and second well regions are a polarity different than the third well region.

10. (Original) The semiconductor device of claim 1, wherein the first and second charge storage layers comprise discrete storage elements.

11-23. (Canceled)